Dipole Engineered Gate Stacks in Ga-Doped In_2O_3 MOSFETs to Enable 1T1C NVDRAM

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Non-volatile memory technology based on ferroelectric material $Hf_{0.5}Zr_{0.5}O_2$ (HZO) have emerged as potential candidates for future random-access memory (RAM) to achieve near or improved performance to DRAM. Of particular interest is the one-transistor-one-capacitor non-volatile DRAM architecture (1T1C NVDRAM) due to its energy efficiency, scalability, and CMOS compatibility [1-4]. Moreover, amorphous oxide semiconductor (AOS) channels such as gallium doped indium oxide have risen as a prospective option for the access transistor due to their BEOL compatibility, very low leakage current, and excellent electrostatic control [5-7]. However, oxide semiconductor FETs (OSFETs) suffer from poor device reliability and fail to operate as enhancement mode devices, which can lead to retention failure. To overcome these challenges without sacrificing performance, we demonstrate dipole engineered gate stacks with a thin Al_2O_3 layer to positively shift the V_T and reduce the threshold voltage shifts (ΔV_T) under positive and negative bias stress.

The process flow for long channel back-gated FETs begins with e-beam evaporation of 20nm Pd and lift-off on a Si/SiO_2 substrate. The dipole engineered gate stacks (Fig. 1) along with a CET matched control (4nm HfO_2) are deposited at 250C via PEALD. The IGO channel was deposited by PEALD at 250C and an engineered super cycle was used to obtain 12% Ga doping and channel thickness of ~ 4nm. Next, 40nm Pd is e-beam evaporated and lifted-off for source drain. Finally, the channel is defined via ICP etching with Cl_2 plasma.

To analyze the effect of the interfacial dipole, the V_T was extracted at a constant current level of 10^{-7} A/μm from the transfer characteristic plots (Fig. 2a). From a statistical analysis of 10 devices for each split, split 2 showed a V_T shift of +270mV relative to the control sample without sacrificing performance. The on current is maintained at ~ 245 μA/μm at an overdrive voltage of 1.5V, which other traditional methods fail to do [6-12]. The positive V_T shift can be explained by the movement of oxygen atoms (and corresponding oxygen vacancies) due to a difference in the oxygen areal density at the metal oxide interface [10]. On the other hand, for bias stability characterization, the ΔV_T is measured over 1000 seconds of stress followed by 1000 seconds of recovery for a range of overdrive field intensities. From the ΔV_T plots (Fig. 2b), split 3 shows improved PBS and NBS with the inserted Al_2O_3 layer. The improved bias stability is attributed to the Al_2O_3 acting as an effective barrier to oxygen vacancy migration under bias stress. Therefore, it has been shown that dipole engineered gate stacks can be used to positively shift the V_T of OSFETs while also improving the stability of the device. Hence, dipole engineering can be used to help enable 1T1C NVDRAM by pushing OSFETs towards enhancement mode and more reliable devices.

References

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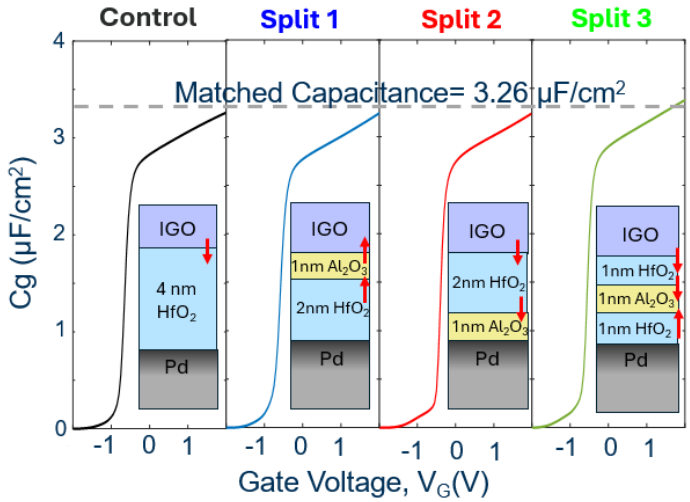

Fig. 1. Capacitance vs voltage for control and splits 1-3. The high-k thickness for the control is set such that it has a matched max capacitance with splits 1-3. The dipole direction is shown in red.

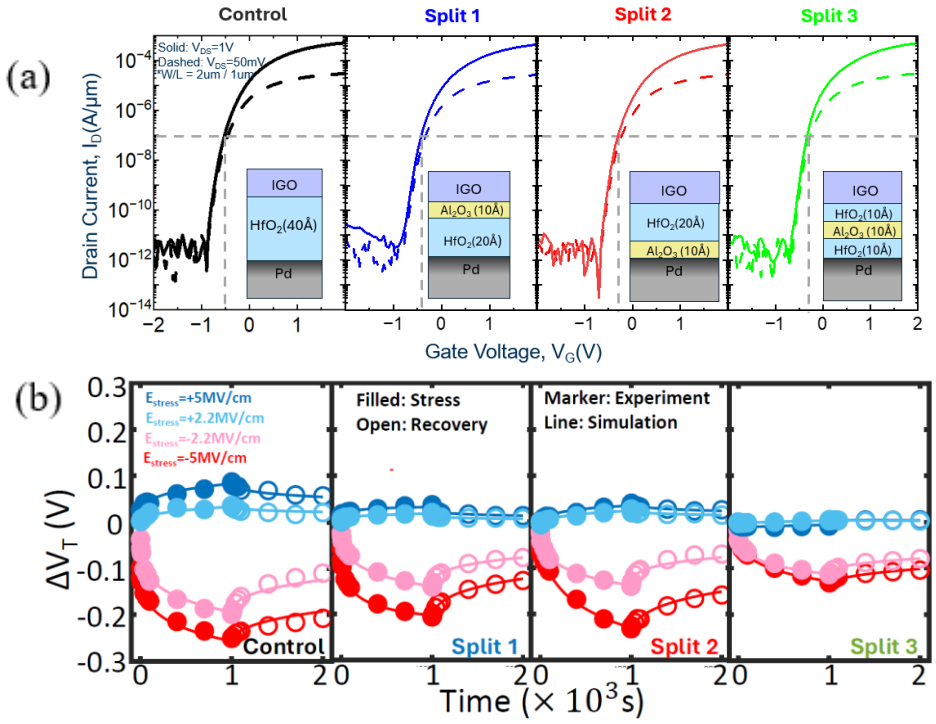

Fig. 2. (a) Transfer characteristics of control and splits 1-3 show VT modulation without degrading on current. (b) NBS and PBS for control and splits 1-3, split 3 shows improved bias stability.

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